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Examiner James C. Kerveros, Art Unit 2133	U.S. Patent & Trademark Office	(571) 272-3824	(571) 273-8300
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**APPLICANTS:** Jae-Woo Roh, et al.**SERIAL NO.:** 10/083,869**FILED:** February 25, 2002**FOR:** HIGH CODE RATE BLOCK CODING/DECODING METHOD AND APPARATUS**ATTORNEY DOCKET NO.:** DE-1344

Dear Examiner Kerveros: Further to our Supplemental Amendment we filed via facsimile on September 8, 2005, kindly replace page 25 of the specification with the attached page, showing the word "of" as deleted in lines 5 and 6.

Thank you very much.

is ensured that seven weighted blocks having smaller summation result in the coding group BG2 are A type weighted blocks while four weighted blocks having larger summation results in the coding group BG2 are B type weighted blocks.

Meanwhile, each of the weighted blocks BB2-2 to BB2-12 produces a reference bit. Since a bit of "1" corresponds to an A type weighted block while a bit of "0" corresponds to a B type weighted block, the coding group BG2 can be represented as a sequence of reference bits 11101001011. This is equal to the bit sequence of the second reference block RB2. Therefore, it will become apparent to those skilled in the art that the second reference block RB2 can be reconstructed in the block decoding system and all the weighted blocks BB2-1 to BB2-12 can be decoded as the original blocks 0B2-1 to 0B1-12.

Hereinafter, the block coding and decoding system for the second preferred embodiment of the present invention will be explained.

Fig. 8 presents a block diagram for illustrating a 20 block coding system in accordance with the second preferred embodiment of the present invention. The block coding system includes an analog-to-digital converter (ADC) 41, a buffering device 43, a first switch 45, a control device 47, an A type coding device 49, a B type coding device 51, a second switch and a third switch 55.

The ADC 41 digitizes an input image signal and provides